CHAPTER - 8

THE ENHANCEMENT-TYPE MOSFET

The p-channel MOSFET is fabricated like a p-channel depletion-type metal-oxide-semiconductor field-effect transistor but without a channel. The p-channel is created when the transistor is properly biased. Such a transistor is referred to as an **enhancement mode p-channel MOSFET** or simply **PMOS**. Let us now examine the construction of a p-channel MOSFET or a PMOS.

8.1 Fabrication of a PMOS

The fabrication of a p-channel MOSFET begins with a base (usually called the substrate) that is highly resistive n-type semiconductor. The base forms the body of the transistor. Diffused into the body are two low-resistivity p-type regions that are separated by the n-type substrate as shown in **Figure 8.1**. Just like any other FET, one of the two p-regions is called the **drain** and the other is the **source.**

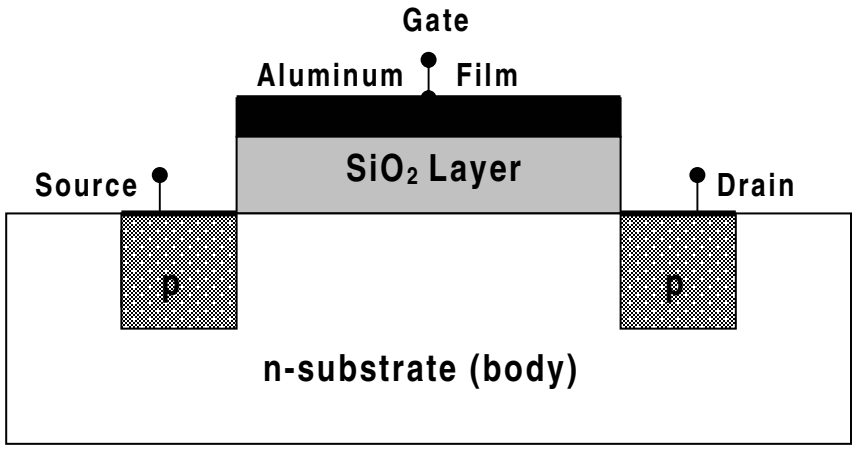

Figure 8.1: Structure of an PMOS

For the formation of the gate, a thin layer of silicon dioxide is grown over the surface of the n-type substrate. A thin film of aluminum is deposited over the insulating layer of silicon dioxide. The aluminum film then acts as the gate terminal as shown. By now you must have realized the absence of the p-channel. It is not created as part of the device. As the n-substrate separates the two p-type regions, there is a very high resistance between the drain and the source. Unless it is properly biased, the device is in its cut-off mode**. For this reason, it is also referred to as a normally OFF device**. On the other hand, the JFET and the DFET are both normally ON devices due to the presence of the channel between the drain and the source terminals.

The thin SiO_2 insulating layer is about 1500 Å. The total chip area required for the fabrication of a FET is less than 5 square mils (1 mil = one-thousandth of an inch). Just for the comparison purposes, about 10 times more chip area is need to manufacture a BJT. This is the main reason for the widespread use of FETs in the fabrication of integrated circuits (ICs).

8.2 Operation of a PMOS

In the fabrication of a PMOS transistor, the gate is insulated from the channel. Therefore, the gate current is negligible regardless of the gate voltage with respect to the source. For this reason, the PMOS is also referred to as an **Insulated Gate Field-Effect Transistor (IGFET).**

Let us first imagine that the drain and the source terminals are held at a common potential as shown in **Figure 8.2**. As the gate terminal is insulated from the channel by the silicon dioxide layer, let us apply a **negative voltage** at the gate with respect to the source. The application of the negative voltage at the gate with respect to the source (V_{GS}) pulls holes into the region between the drain and the source and pushes away the electrons. This is due to the capacitor formed by the insulating SiO_2 layer between the gate and the p-type substrate. As V_{GS} is made more and more negative, more and more holes (positive

charges) are attracted toward the gate. These positive charges redistribute themselves in the region between the drain and the source in the form of a thin layer. This layer of excess positive charges is called a **p-type inversion layer**. As soon as V_{GS} reaches a **threshold voltage** (V_T), the entire region between the drain and the source gets filled with the positive charges. Thus, **a channel has been induced in the n-region just below the gate**. The channel now connects the drain to the source. As a result, the conductivity of the region between the drain and the source increases which, in turn, allows the current to flow from the source toward the drain when drain is held at a lower potential than the source. Any further decrease in V_{GS} widens the channel and further increases its conductivity. This, in turn, increases the drain current (Note that the current enters at the source, flows through the channel, and exits at the drain).

The drain current continues to increase with the decrease in the gate-to-source voltage. Since the negative gate voltage increases (enhances) the channel's conductivity, the **PMOS is said to operate in its enhancement mode when the gate is negative with respect to the source**. We can also say that the **PMOS operates in the enhancement mode when the source is positive with respect to the gate**.

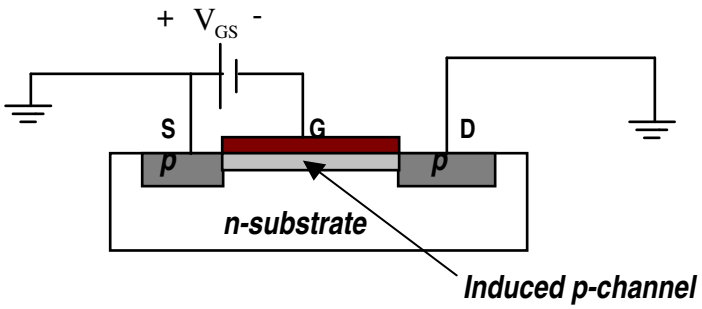

Figure 8.2 Induced n-channel in a PMOS

Let us now apply a negative voltage at the drain with respect to the source (V_{DS}) as shown in **Figure 8.3** while the gate-to-source voltage, V_{GS}, is less than V_T, where V_T is a negative voltage. As soon as V_{DS} becomes less than zero, there is a current (I_D) from the source toward the drain through the highly conductive channel. However, with the decrease in V_{DS} (or increase in V_{SD}), the gate-to-drain voltage increases which, in turn, results in the decrease in channel's width near the drain terminal. The channel's width near the source terminal remains the same as long as V_{GS} is held constant. The decrease in channel's width near the drain causes a decrease in its conductivity and an increase in its resistance. As long as the channel exists between the drain and the source, the drain current increases with the decrease in the drain-to-source voltage**. This is the linear (or triode) region of operation of the PMOS.**

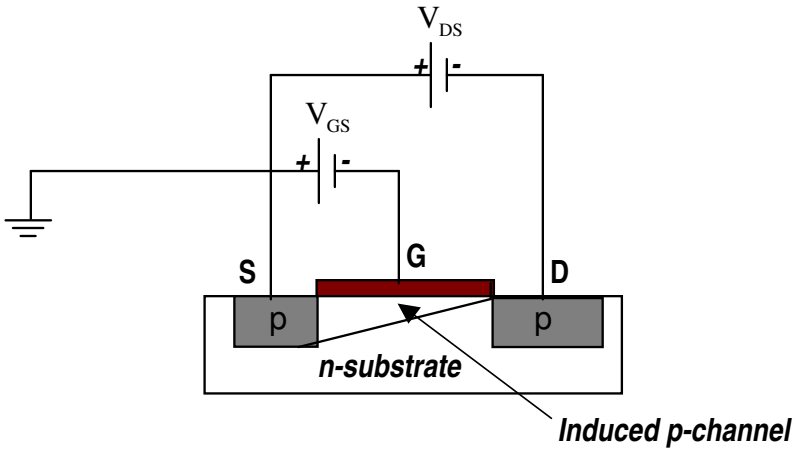

Figure 8.3 Channel modulation of a PMOS (when $V_{SD} = V_{SDP}$)

As we continue to decrease V_{DS} (or increase V_{SD}), the channel's width near the drain continues to diminish until it pinches off as shown in **Figure 8.3**. This process is commonly referred to as **channel modulation**. At the pinch-off point, the drain-to-source voltage is referred to as the drain-to-source pinch-off voltage V_{DSP}, which is a negative quantity. However, we can refer to it as the source-to-drain pinch-off voltage (V_{SDP}) and then it would be a positive quantity. The channel's width near the drain is almost zero and the channels resistance becomes very high (almost infinite). Any further decrease in the drain-to-source voltage V_{DS} (or increase in the source-to-drain voltage, V_{SD}) does not result in any appreciable increase in the drain current. The device has entered the **saturation region**. In this region, $V_{SD} \geq V_{SDP}$. Note that V_{SD} and V_{SDP} are both positive voltages, where V_{SD} is the applied source-to-drain voltage and V_{SDP} is the source-to-drain pinch-off voltage.

As V_{DS} is decreased beyond V_{DSP} (or V_{SD} is increased beyond V_{SDP}), the drain current remains almost constant but the channel modulation continues and the pinch-off point moves toward the source as illustrated in **Figure 8.4**. The transistor continues to operate in the saturation region as long as V_{SD} is less than the breakdown voltage of the device.

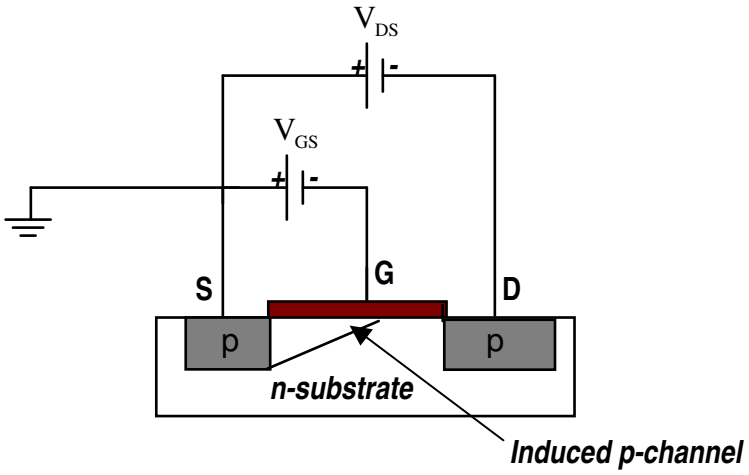

Figure 8.4: Pinch-off point as a function of V_{SD} (when $V_{SD} > V_{SDP}$)

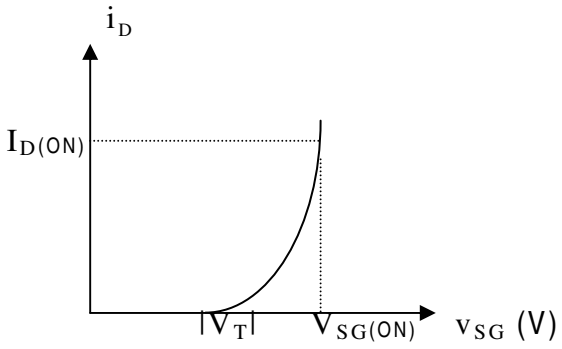

Figure 8.5: Transfer characteristic of a PMOS

8.3 Various Characteristics of a PMOS

The **transfer characteristic** of a PMOS is given in **Figure 8.5** where its threshold voltage is V_T (where V_T is a negative voltage). The data sheet on the transistor usually provides information on the threshold voltage and another point on the curve as shown.

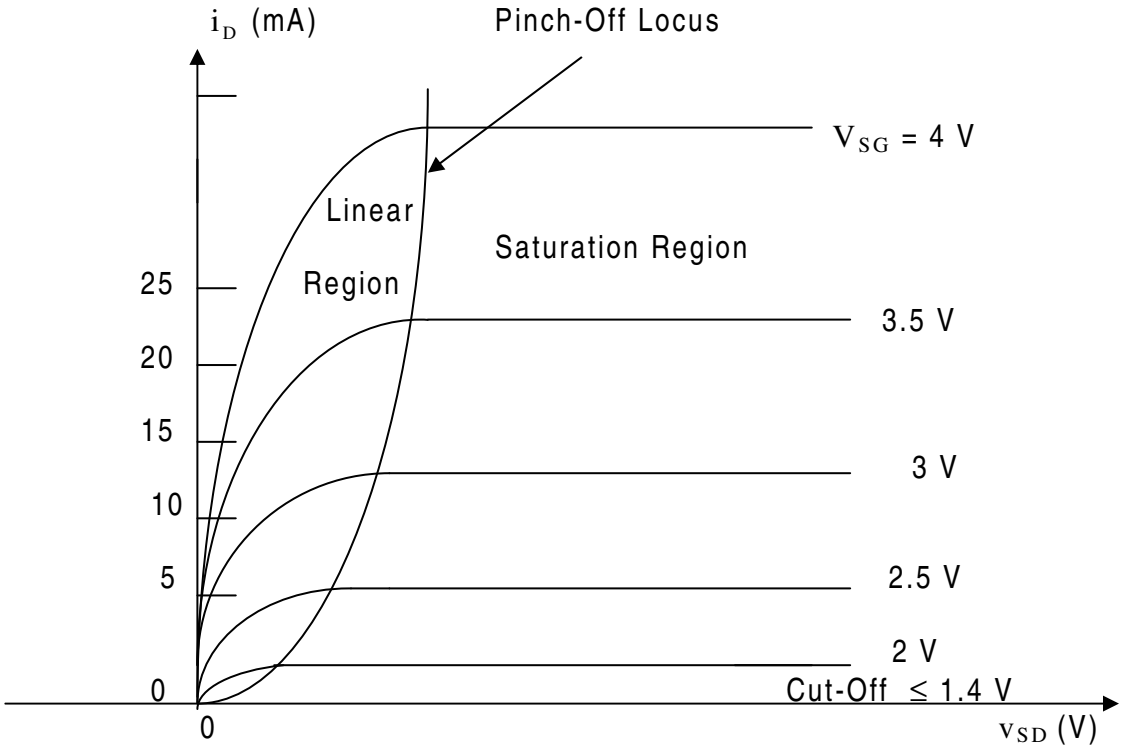

Figure 8.6: Drain current family of characteristics of a PMOS

A typical family of drain current characteristics (v_{SD} vs. i_D) is given in **Figure 8.6** for a PMOS. Note that the drain current is almost zero for $V_{SG} \leq |V_T|$, where V_T is about -1.4 V.

8.4 Schematic diagrams for a PMOS

The four-terminal schematic diagram for the p-channel MOSFET is given in **Figure 8.7a.** The solid line for the gate is separated by a broken line that shows the connections for the drain and the source. The space between the solid and the broken lines is for the channel and the broken line indicates its absence. In other words, the channel is yet to be induced. The arrow on the substrate points from the p-channel toward the n-type substrate. The fabrication of the device creates a pnp transistor (not shown) where drain is the collector, substrate is the base, and the source is the emitter.

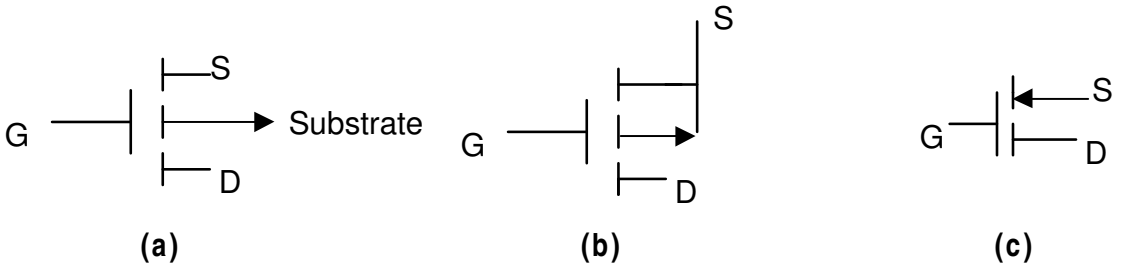

Figure 8.7: Various symbols for a PMOS.

In most applications, the source and the substrate are connected together. In fact, the manufacturer of the device may have already done it. The schematic for the three-terminal device is shown in **Figure 8.7b**. The pnp transistor (not shown) now acts as a reverse biased diode when the source is positive with respect to the drain. This parasitic diode is a blessing in disguise when the transistor is used as a switch.

A somewhat simplified symbol, **Figure 8.7c,** is also used where the broken line between the drain and the source further stresses the absence of the channel. The arrow now points in the direction of the current flow into the source terminal. Once again, the current enters the device at the source and exits at the drain after passing through the channel. **In order to be consistent with our nomenclature for the NMOS transistor, we will still refer to it as the drain-to-source current.**

8.5 BIASING OF A PMOS

Since a PMOS operates like any other transistor we have discussed so far, it can be biased using the same biasing schemes. The PMOS can only be turned ON by applying a negative voltage at the gate with respect to the source. The gate-to-source voltage must be less than its threshold voltage. The P-DFET, on the other hand, has an advantage over the PMOS in the sense that it can be biased at the point where gate-to-source voltage is zero.

The PMOS enters the cut-off mode as soon as its gate-to-source voltage becomes equal or greater than its threshold voltage. Keep in mind that for a PMOS, the threshold voltage is less than zero. For example, the typical value of the threshold voltage may be about – 1.0 V. In order to make the equations for the PMOS transistors to look exactly like those for the NMOS transistor (see previous section), we will use the absolute value of the threshold voltage.

8.6 EQUATIONS FOR A PMOS

The appropriate equations for a PMOS are usually given in terms of the conduction parameter K_P. The conduction parameter depends upon the fabrication of a PMOS. It has been theoretically determined that K_P is a function of the length and width of the channel, the mobility of the major charge carriers in the channel, and thickness of the SiO_2 layer.

In the equation form, K_P is given as

$$K_P = \frac{1}{2}\mu_p C_{ox} \frac{W}{L} = \frac{k_P}{2}\frac{W}{L}$$

where μ_p is the mobility of the holes in the p-channel, W is the width and L is the length of the channel, and C_{ox} is the capacitance per unit area of the SiO_2 layer. If ε_{ox} is the permittivity of the SiO_2 layer and t_{ox} is its thickness, then the capacitance per unit area of the SiO_2 layer is

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \quad (F/m^2)$$

The parameter $k_p = \mu_p C_{ox}$ is usually a constant quantity. Therefore, the conduction parameter K_P is directly proportional to the width and is inversely proportional to the length of the channel. The details of SiO_2 layer and the dimensions of the p-channel (below the layer) are shown in **Figure 8.8.**

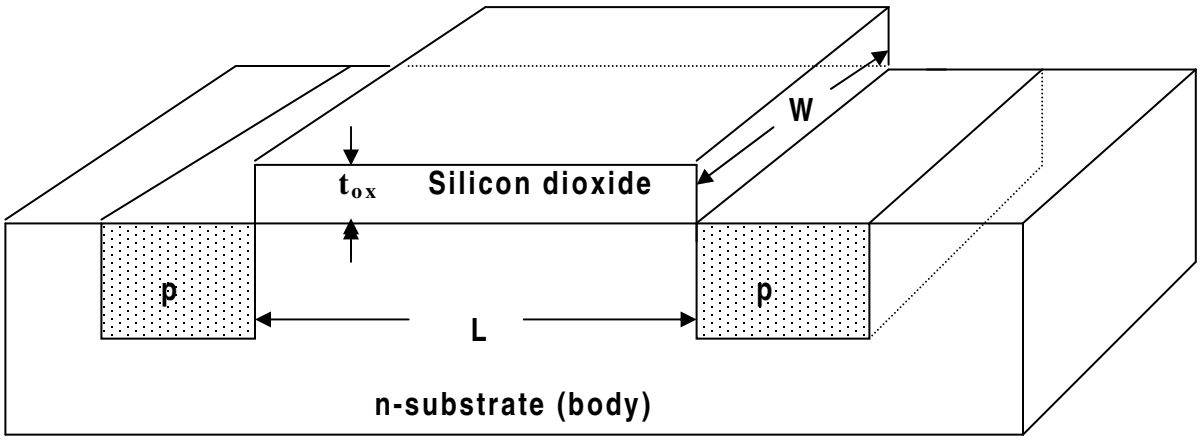

Figure 8.8: Details of SiO_2 layer

Equations for a PMOS

(a) Cut-off Region

$$v_{SG} \leq |V_T| \quad \text{where} \quad V_T < 0$$

$$i_D = 0$$

(b) Operation in the Saturation Region:

$$V_{SDP} = v_{SG} - |V_T|$$

Condition: $v_{SD} \geq V_{SDP}$

$$i_D = K_P \left(v_{SG} - |V_T|\right)^2$$

where $$K_P = \frac{1}{2} \mu_p C_{ox} \frac{W}{L} = k_P' \frac{W}{L}$$

and $$k_P' = \frac{1}{2} \mu_P C_{ox}$$

Transconductance: For small-signal analysis

$$g_m = 2\sqrt{K_P I_{DQ}}$$

(c) Operation in the Linear (Triode or Ohmic) Region:

$$V_{SDP} = v_{SG} - |V_T|$$

Condition: $v_{SD} < V_{SDP}$

$$i_D = 2 K_P \left[v_{SG} - |V_T| - 0.5\, v_{SD}\right] v_{SD}$$

where $$K_P = \frac{1}{2} \mu_p C_{ox} \frac{W}{L} = k_P' \frac{W}{L}$$

and $$k_P' = \frac{1}{2} \mu_P C_{ox}$$

Example 8.1: PMOS Amplifier _____

A common-gate amplifier using a PMOS transistor is given in **Figure 8.9**. The parameters for the transistor are K_P = 0.5 mA/V², and V_T = – 1 V. The other parameters are R_S = 2 kΩ, R_D = 4 kΩ, R_G = 100 kΩ, R_L = 4 kΩ, and the internal resistance of the input signal is r_s = 0.5 kΩ Determine its Q-point. Also obtain its voltage, current and power gains. What are the input and output resistances?

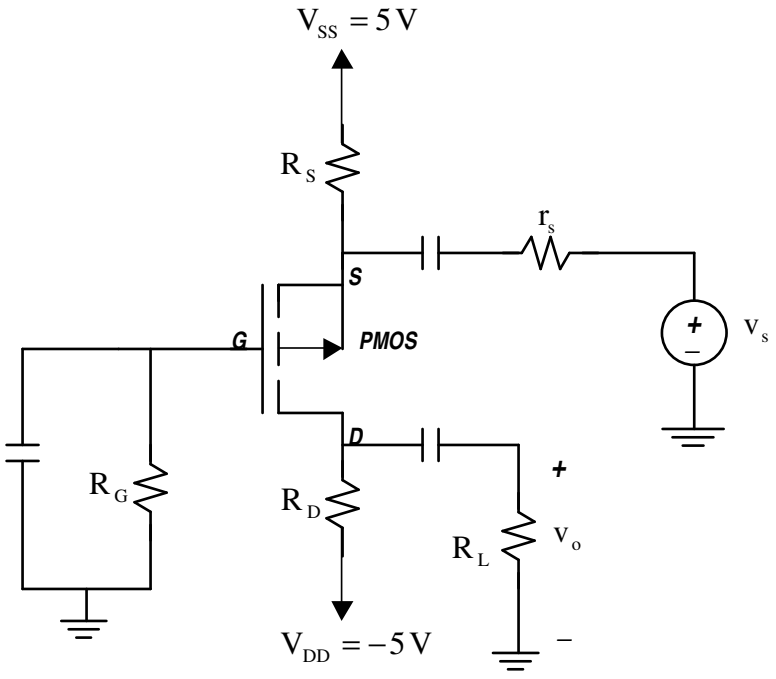

Figure 8.9: Common-gate PMOS amplifier

DC Analysis

For the following analysis, all resistors are in kΩ and all currents are in mA unless it is mentioned otherwise.

The gate voltage is zero. That is, V_G = 0

Let I_D be the current in the transistor, then the voltage at the source terminal is

$$V_S = V_{SS} - I_D R_S = 5 - 2 I_D$$

The source-to-gate voltage: $V_{SG} = V_S - V_G = 5 - 2 I_D$

Assuming that the PMOS transistor operates in the saturation region, the current in the transistor can be computed as

$$I_D = K_P (V_{SG} - |V_T|)^2 = 0.5 (5 - 2 I_D - 1)^2$$

The solution of this equation yields $I_D = 3.28$ mA or $I_D = 1.22$ mA. The drain current cannot be 3.28 mA because it forces the transistor to operate in the cut-off region. Therefore, the only viable solution for the drain current is 1.22 mA. For $I_D = 1.22$ mA, the source terminal voltage and the source-to-gate voltages are

$$V_S = 5 - 2 \times 1.22 = 2.56 \text{ V}$$

$$V_{SG} = 5 - 2 \times 1.22 = 2.56 \text{ V}$$

The voltage at the drain terminal is

$$V_D = R_D I_D - 5 = 4 \times 1.22 - 5 = -0.12 \text{ V}$$

Thus, the source-to-drain voltage is

$$V_{SD} = V_S - V_D = 2.56 - (-0.12) = 2.68 \text{ V}$$

The source-to-drain voltage at the transition point is

$$V_{SDP} = V_{SG} - |V_T| = 2.56 - |-1| = 1.56 \text{ V}$$

Since V_{SD} is greater than V_{SDP}, the transistor operates in the saturation region and our assumption is correct.

Hence, at the dc operating point, we have

$$I_{DQ} = 1.22 \text{ mA}, \quad V_{SDQ} = 2.68 \text{ V}, \quad \text{and} \quad V_{SGQ} = 2.56 \text{ V}.$$

The transconductance for the small signal analysis is

$$g_m = 2\sqrt{K_P I_{DQ}} = 2\sqrt{0.5 \times 1.22} = 1.562 \text{ mS}$$

Small Signal Analysis

The equivalent circuit for the small signal analysis is given in **Figure 8.10**.

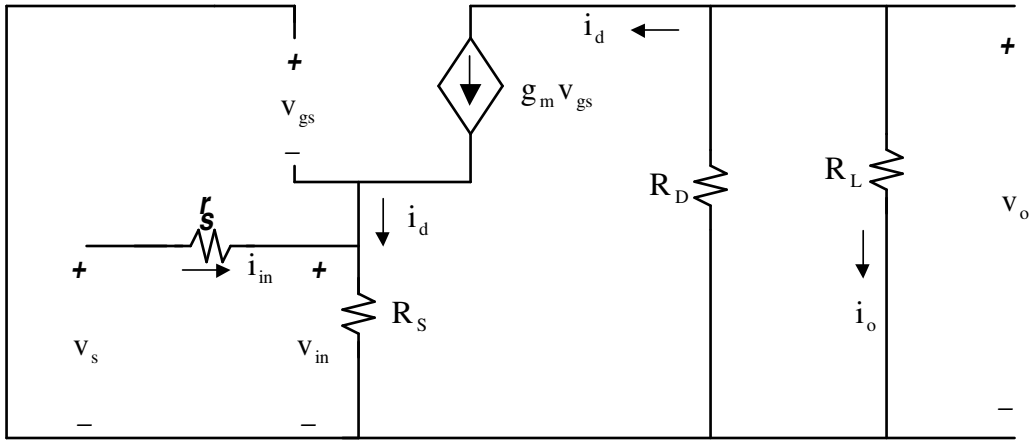

Figure 8.10: Small signal model of the common-gate PMOS amplifier

Let us work out all equations in term of v_{in}, the voltage across R_S. It is evident from the figure that

$$v_{gs} = - v_{in}$$

The small signal current through the transistor is

$$i_d = g_m \, v_{gs} = - g_m \, v_{in}$$

Thus, the output voltage is

$$v_o = - i_d \, R_{ac} = g_m \, R_{ac} \, v_{in} \qquad (8.1)$$

where R_{ac} is the equivalent load resistance. It is the parallel combination of R_D and R_L. That is, $R_{ac} = R_D \, || \, R_L$. Since $R_D = R_L = 4$ kΩ, $R_{ac} = 2$ kΩ. From the above equation it is evident that the output voltage is in phase with the input signal.

We can now determine the voltage gain as

$$A_V = \frac{v_o}{v_{in}} = g_m\ R_{ac} = 1.562 \times 2 = 3.124$$

From the output voltage expression, we can obtain an equation for the output current as

$$i_o = \frac{v_o}{R_L} = \frac{g_m\ R_D}{R_D + R_L}\ v_{in}$$

The input current: $$i_{in} = \frac{v_{in}}{R_S} - i_d = \frac{v_{in}}{R_S} + g_m\ v_{in} = \frac{1 + g_m\ R_S}{R_S}\ v_{in}$$

Thus, the input resistance: $$R_{in} = \frac{v_{in}}{i_{in}} = \frac{R_S}{1 + g_m\ R_S}$$

The current gain: $$A_I = \frac{i_o}{i_{in}} = \frac{g_m\ R_S}{1 + g_m\ R_S}\left(\frac{R_D}{R_D + R_L}\right)$$

Substituting g_m = 1.562 mS, R_S = 2 kΩ, R_D = 4 kΩ, and R_L = 4 kΩ in the above expressions, we obtain

R_{in} = 0.485 kΩ, or 485 Ω

A_I = 0.379

Finally, the power gain: $$A_P = A_V\ A_I = 0.583$$

The output resistance is simply R_D = 4 kΩ.

In order to compute the overall voltage gain, we have to express v_{in} in terms of the input signal v_s as

$$v_{in} = \frac{R_{in}}{R_{in} + r_s}\ v_s$$

Substituting R_{in} = 0.485 kΩ and r_s = 0.5 kΩ, we obtain $v_{in} = 0.492\ v_s$.

Equation (8.1) can now be expressed as

$$v_o = 0.492\ g_m\ R_{ac}\ v_s$$

Thus, the overall gain: $$A_{VS} = \frac{v_o}{v_s} = 0.492\ g_m\ R_{ac} = 0.492 \times 1.562 \times 2 = 1.537$$

8.7 PROBLEMS: PMOS TRANSISTORS

8.1 A **common-source** PMOS amplifier circuit is given in **Figure P8.1**. The transistor parameters are K_P = 0.8 mA/V² and V_T = – 2 V. The resistances in the circuit are R_S = 2 kΩ, R_D = 1.2 kΩ, R_G = 150 kΩ. Determine the dc operating point and sketch the dc and ac load lines. Compute the small-signal voltage gain. If the input voltage varies sinusoidally, sketch the output voltage.

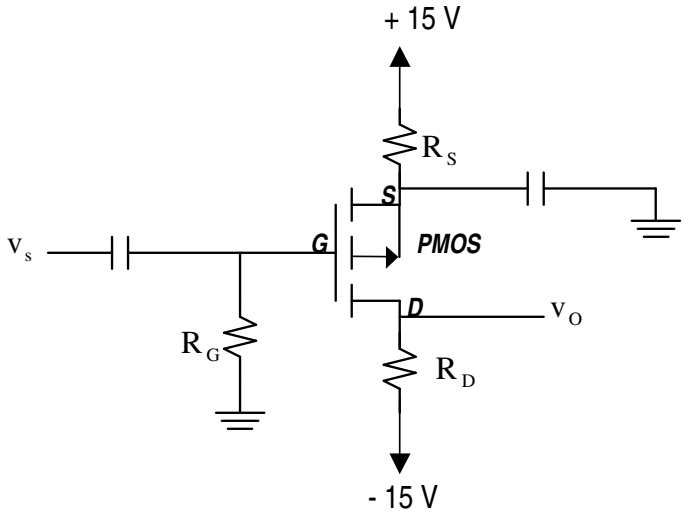

Figure P8.1

8.2 A **common-drain** (**source follower**) PMOS transistor circuit is shown in **Figure P8.2**. The transistor parameters are K_N = 0.5 mA/V² and V_T = – 1 V. The other resistances in the circuit are R_1 = 260 kΩ, R_2 = 40 kΩ, R_L = 200 Ω, and R_S = 2 kΩ. Determine the dc operating point of the transistor. Sketch its dc and ac load lines. Calculate the small-signal voltage, current, and power gains. Compute the input and output resistances.

8.3 Determine the voltage gain of the amplifier shown in **Figure P8.2** when the load resistance is removed. Under ideal conditions, the voltage gain should be unity. What is the percent difference between the ideal and the actual voltage gains?

8.4 Repeat **Problem 8.2** when the input signal has an internal resistance of 2 kΩ. What is the effect of the input resistance on the overall voltage gain of the amplifier? If you were given the liberty to change the circuit components, what would you do to minimize the effect of the source resistance on the voltage gain without changing the dc operating point?

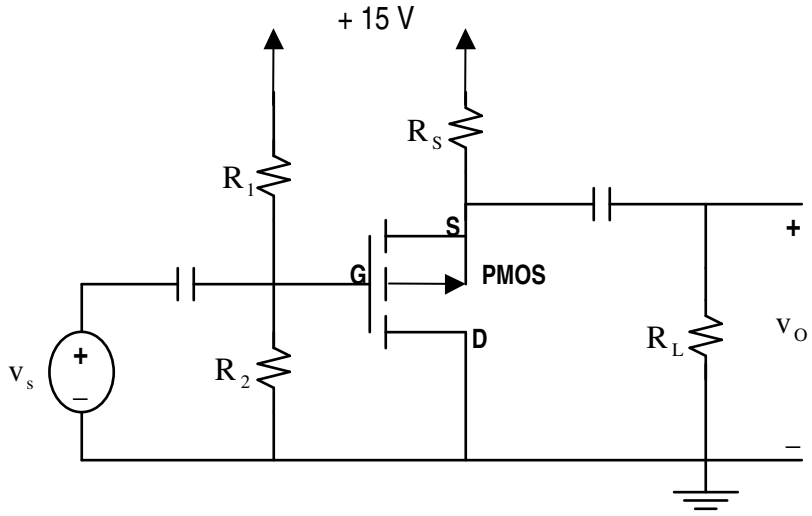

Figure P8.2

8.5 A common-gate PMOS amplifier is given in **Figure P8.5**. The transistor parameters are K_N = 0.5 mA/V² and V_T = – 1 V. The other resistances in the circuit are R_1 = 120 kΩ, R_2 = 80 kΩ, R_D = 1 kΩ, and R_S = 1.5 kΩ. Determine the voltage, current, and power gains. Also compute the input and the output resistances.

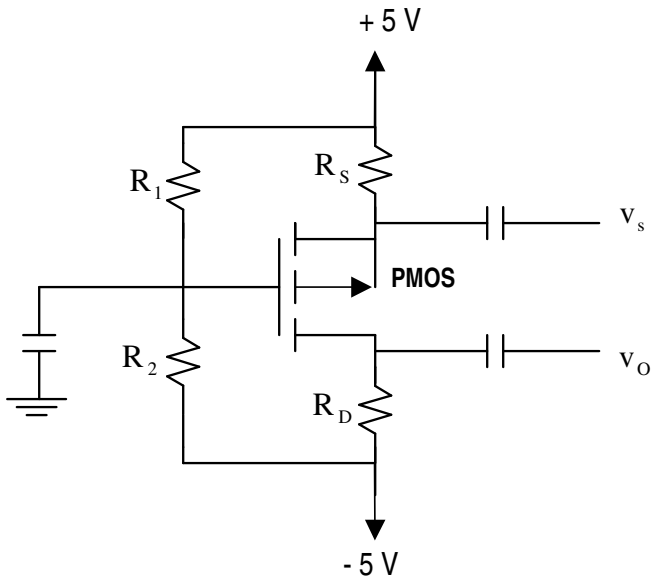

Figure P8.5